



Intel® Celeron® D Processor 300^Δ Sequence

Specification Update

– On 65 nm Process in the 775-land LGA Package

Oct 2006 “OOC”

Notice: The Intel® Celeron® D Processor 300 Sequence on 65 nm process may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.



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XD denotes Execute Disable Bit. Enabling Execute Disable Bit functionality requires a PC with a processor with Execute Disable Bit capability and a supporting operating system. Check with your PC manufacturer on whether your system delivers Execute Disable Bit functionality.

The Intel® Celeron® D Processor on 65 nm process may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Φ Intel® 64 requires a computer system with a processor, chipset, BIOS, operating system, device drivers, and applications enabled for Intel 64. Processor will not operate (including 32-bit operation) without an Intel 64-enabled BIOS. Performance will vary depending on your hardware and software configurations. See <http://www.intel.com/info/em64t> for more information including details on which processors support Intel 64, or consult with your system vendor for more information.

^AIntel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. Over time processor numbers will increment based on changes in clock, speed, cache, FSB, or other features, and increments are not intended to represent proportional or quantitative increases in any particular feature. Current roadmap processor number progression is not necessarily representative of future roadmaps. See www.intel.com/products/processor_number for details.

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Contents

| | |
|------------------------------------|----|
| Revision History | 4 |
| Preface | 5 |
| Summary Tables of Changes | 7 |
| Identification Information | 10 |
| Errata | 12 |
| Specification Changes | 22 |
| Specification Clarifications | 23 |
| Documentation Changes | 24 |

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Revision History

| Revision | Description | Date |
|----------|--|--------------------------|
| -001 | <ul style="list-style-type: none">Initial release of the Intel® Celeron® D Processor 300 Sequence Specification Update | May 2006 Out of Cycle |
| -002 | <ul style="list-style-type: none">Added Erratum AD23, AD24 and AD25. | June 2006 |
| -003 | <ul style="list-style-type: none">Added R_{TT} Specification Change | July 2006 |
| -004 | <ul style="list-style-type: none">Added D step information. Added information for processor number 360 | Aug 2006 Out Of Cycle |
| -005 | <ul style="list-style-type: none">Added Specification change AD1. | Oct 2006 |
| -006 | <ul style="list-style-type: none">Added information for processor number 347. | Oct 2006 Out of Cycle |

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents and Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools.

Information types defined in the Nomenclature section are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

| Document Title | Document Number |
|--|-----------------|
| <i>Intel® Celeron® D Processor 300 Sequence Datasheet – On 65 nm Process in the 775-Land LGA Package</i> | 311826 |

Related Documents

| Document Title | Document Location |
|---|---|
| <i>IA-32 Intel® Architecture Software Developer's Manual Volume 1: Basic Architecture</i> | http://developer.intel.com/design/pentium4/manuals/index_new.htm |
| <i>IA-32 Intel® Architecture Software Developer's Manual Volume 2A: Instruction Set Reference Manual A–M</i> | |
| <i>IA-32 Intel® Architecture Software Developer's Manual Volume 2B: Instruction Set Reference Manual, N–Z</i> | |
| <i>IA-32 Intel® Architecture Software Developer's Manual Volume 3A: System Programming Guide</i> | |
| <i>IA-32 Intel® Architecture Software Developer's Manual Volume 3B: System Programming Guide</i> | |



Nomenclature

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics (e.g., core speed, L2 cache size, package type, etc.) as described in the processor identification information table. Care should be taken to read all notes associated with each S-Spec number

QDF Number is a several digit code that is used to distinguish between engineering samples. These processors are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. The NDA specification update has a processor identification information table that lists these QDF numbers and the corresponding product sample details.

Errata are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed component steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

| | |
|---------------------------|---|
| X: | Erratum, Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank Box): | This erratum is fixed in the listed stepping or specification change does not apply to the listed stepping. |

Status

| | |
|----------|--|
| Doc: | Document change or update that will be implemented. |
| PlanFix: | This erratum may be fixed in a future stepping of the product. |
| Fixed: | This erratum has been previously fixed. |
| NoFix: | There are no plans to fix this erratum. |
| Shaded: | This item is either new or modified from the previous version of the document. |

Note: Each Specification Update item is prefixed with a capital letter to distinguish the product. The key below details the letters that are used in Intel's microprocessor Specification Updates:

- A = Intel® Pentium® II processor
- B = Mobile Intel® Pentium® II processor
- C = Intel® Celeron® processor
- D = Intel® Pentium® II Xeon® processor
- E = Intel® Pentium® III processor
- F = Intel® Pentium® processor Extreme Edition
- G = Intel® Pentium® III Xeon® processor
- H = Mobile Intel® Celeron® processor at 466 MHz, 433 MHz, 400 MHz, 366 MHz, 333 MHz, 300 MHz, and 266 MHz
- K = Mobile Intel® Pentium® III Processor – M
- L = Intel® Celeron® D processor

M = Mobile Intel® Celeron® processor
 N = Intel® Pentium® 4 processor
 O = Intel® Xeon® processor MP
 P = Intel® Xeon® processor
 Q = Mobile Intel® Pentium® 4 processor supporting Hyper-Threading Technology on 90-nm process technology
 R = Intel® Pentium® 4 processor on 90 nm process
 S = 64-bit Intel® Xeon® Processor with 800 MHz system bus
 T = Mobile Intel® Pentium® 4 processor – M
 U = 64-bit Intel® Xeon® processor MP with up to 8MB L3 Cache
 V = Mobile Intel® Celeron® processor on 0.13 Micron Process in Micro-FCPGA Package
 W = Intel® Celeron® M processor
 X = Intel® Pentium® M processor on 90 nm process with 2-MB L2 cache
 Y = Intel® Pentium® M processor
 Z = Mobile Intel® Pentium® 4 processor with 533 MHz system bus
 AA = Intel® Pentium® processor Extreme Edition and Intel® Pentium® D processor on 65nm process
 AB = Intel® Pentium® 4 processor 6x1 Sequence
 AC = Intel® Celeron® processor in 478 pin package
 AD = Intel® Celeron® D processor 300 Sequence
 AE = Intel® Core™ Duo Processor and Intel® Core™ Solo processor on 65nm process

| NO | B1 | C1 | D0 | Plan | ERRATA |
|------|----|----|----|--------|--|
| AD1 | X | X | X | No Fix | Memory Aliasing of Pages as Uncacheable Memory Type and Write Back (WB) May Hang the System |
| AD2 | X | X | X | No Fix | Data Breakpoints on the High Half of a Floating Point Line Split may not be Captured |
| AD3 | X | X | X | No Fix | MOV CR3 Performs Incorrect Reserved Bit Checking When in PAE Paging |
| AD4 | X | X | X | No Fix | Incorrect Access Controls to MSR_LASTBRANCH_0_FROM_LIP MSR Registers |
| AD5 | X | X | X | No Fix | FXRSTOR May Not Restore Non-canonical Effective Addresses on Processors with Intel® 64 architecture Enabled |
| AD6 | X | X | X | No Fix | A Push of ESP that Faults may Zero the Upper 32 Bits of RSP |
| AD7 | X | X | X | No Fix | Checking of Page Table Base Address May Not Match the Address Bit Width Supported by the Platform |
| AD8 | X | X | X | No Fix | With TF (Trap Flag) Asserted, FP Instruction That Triggers an Unmasked FP Exception May Take Single Step Trap Before Retirement of Instruction |
| AD9 | X | X | X | No Fix | BTS(Branch Trace Store) and PEBS(Precise Event Based Sampling) May Update Memory outside the BTS/PEBS Buffer |
| AD10 | X | X | X | No Fix | Control Register 2 (CR2) Can be Updated during a REP MOVS/STOS Instruction with Fast Strings Enabled |
| AD11 | X | X | X | No Fix | REP STOS/MOVS Instructions with RCX $\geq 2^{32}$ May Cause a System Hang |
| AD12 | X | X | X | No Fix | A 64-Bit Value of Linear Instruction Pointer (LIP) May be Reported Incorrectly in the Branch Trace Store (BTS) Memory Record or in the Precise Event Based Sampling (PEBS) Memory Record |

| NO | B1 | C1 | D0 | Plan | ERRATA |
|------|----|----|----|--------|---|
| AD13 | X | X | X | No Fix | Two Correctable L2 Cache Errors in Close Proximity May Cause a System Hang |
| AD14 | X | X | X | No Fix | Processor May Hang with a 25% or Less STPCLK# Duty Cycle |
| AD15 | X | X | X | No Fix | Machine Check Exceptions May not Update Last-Exception Record MSRs (LERs) |
| AD16 | X | X | X | No Fix | Writing the Local Vector Table (LVT) when an Interrupt is Pending May Cause an Unexpected Interrupt |
| AD17 | X | X | | Fixed | At a Bus Ratio of 13:1, RCNT and Address Parity May be Incorrect |
| AD18 | X | X | X | No Fix | IRET under Certain Conditions May Cause an Unexpected Alignment Check Exception |
| AD19 | X | X | X | No Fix | L2 Cache ECC Machine Check Errors May be erroneously Reported after an Asynchronous RESET# Assertion |
| AD20 | X | X | X | No Fix | Using 2M/4M Pages When A20M# Is Asserted May Result in Incorrect Address Translations |
| AD21 | X | X | X | No Fix | Writing Shared Unaligned Data that Crosses a Cache Line without Proper Semaphores or Barriers May Expose a Memory Ordering Issue |
| AD22 | X | X | X | No Fix | The IA32_MC0_STATUS and IA32_MC1_STATUS Overflow Bit is not set when Multiple Un-correctable Machine Check Errors Occur at the Same Time |
| AD23 | X | X | X | No Fix | Processor May Fault When the Upper 8 Bytes of Segment Selector Is Loaded from a Far Jump through a Call Gate via the Local Descriptor Table |
| AD24 | X | X | X | No Fix | The Processor May Issue Front Side Bus Transactions up to 6 Clocks after RESET# is Asserted |
| AD25 | X | X | X | No Fix | Front Side Bus Machine Checks May be Reported as a Result of On-Going Transactions during Warm Reset |

| No. | Plan | SPECIFICATION CHANGES |
|-----|------|-------------------------------------|
| AD1 | DOC | VTT_SEL Signal Specification change |

| No. | Plan | SPECIFICATION CLARIFICATIONS |
|-----|------|--|
| | | There are no Specification Clarifications in this Specification Update revision. |

| NO. | Plans | DOCUMENTATION CHANGES |
|-----|-------|---|
| | | There are no Documentation Changes in this Specification Update revision. |

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Identification Information

Figure 1. Intel® Celeron® D Processor 300 sequence Package supporting 775_VR_CONFIG_05A Specifications (Top Markings for C1 stepping)

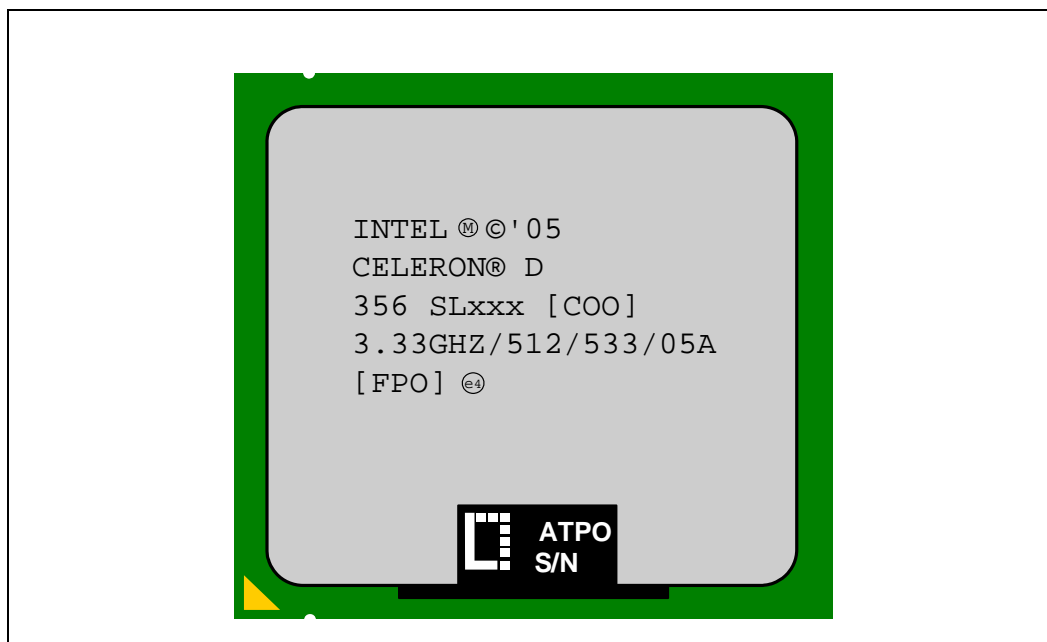
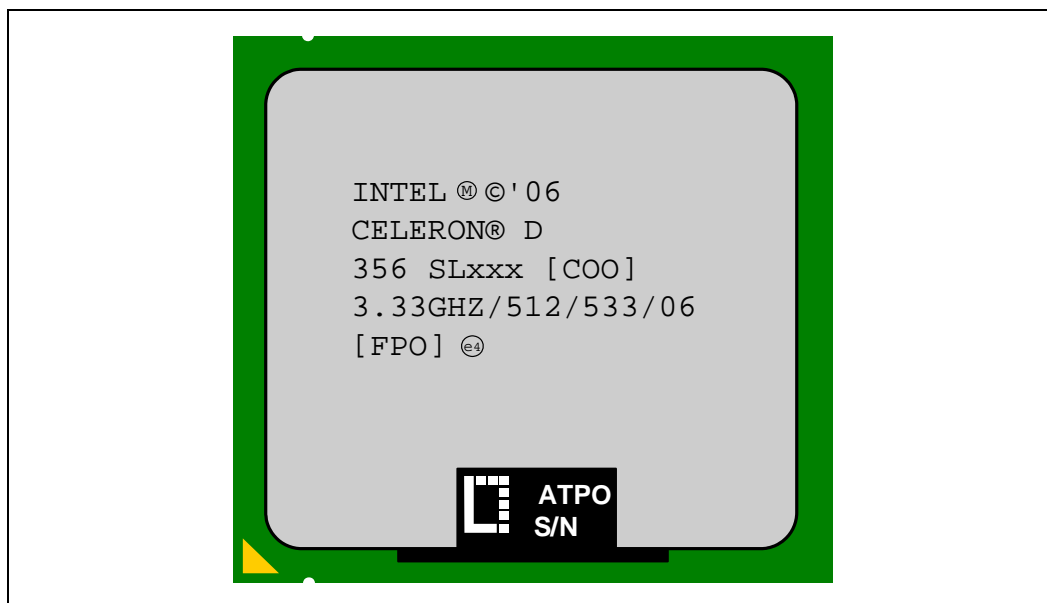


Figure 2. Intel® Celeron® D Processor 300 sequence Package supporting 775_VR_CONFIG_06 Specifications (Top Markings for D0 stepping)



Component Identification Information

The Intel® Celeron® D Processor on 65 nm process can be identified by the following values:

| Family ¹ | Model ² |
|---------------------|--------------------|
| 1111b | 0110b |

NOTES:

1. The Family corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
2. The Model corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register. Refer to the *Intel Processor Identification and the CPUID Instruction Application Note* (AP-485) and the *Cedar Mill Processor Family BIOS Writer's Guide (BWG)* for further information on the CPUID instruction.

Table 1. Intel® Celeron® D Processor 300 Sequence Identification Information

| S-Spec | Core Stepping | L2 Cache Size (bytes) | Processor Signature | Processor Number | Speed Core/Bus | Package | Notes |
|--------|---------------|-----------------------|---------------------|------------------|------------------|--------------|---------|
| SL9XU | C1 | 512K | 0F64h | 347 | 3.06 GHz/533 MHz | 775-land LGA | 1, 3, 4 |
| SL96P | C1 | 512K | 0F64h | 352 | 3.20 GHz/533 MHz | 775-land LGA | 1, 3, 4 |
| SL96N | C1 | 512K | 0F64h | 356 | 3.33 GHz/533 MHz | 775-land LGA | 1, 3, 4 |
| SL9KK | D0 | 512K | 0F65h | 360 | 3.6 GHz/533 MHz | 775-land LGA | 2, 3, 4 |

NOTES:

1. These processors support the 775_VR_CONFIG_05A (mainstream) specifications.
2. These processors support the 775_VR_CONFIG_06 specifications.
3. These parts support Intel® 64.
4. These parts support Execute Disable Bit Feature.

Errata

AD1. Memory Aliasing of Pages as Uncacheable Memory Type and Write Back (WB) May Hang the System

Problem: When a page is being accessed as either Uncacheable (UC) or Write Combining (WC) and WB, under certain bus and memory timing conditions, the system may loop in a continual sequence of UC fetch, implicit writeback, and Request For Ownership (RFO) retries.

Implication: This erratum has not been observed in any commercially available operating system or application. The aliasing of memory regions, a condition necessary for this erratum to occur, is documented as being unsupported in the *IA-32 Intel® Architecture Software Developer's Manual*, Volume 3, section 10.12.4, Programming the PAT. However, if this erratum occurs the system may hang.

Workaround: The pages should not be mapped as either UC or WC and WB at the same time.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD2. Data Breakpoints on the High Half of a Floating Point Line Split May Not Be Captured

Problem: When a floating point load which splits a 64-byte cache line gets a floating point stack fault, and a data breakpoint register maps to the high line of the floating point load, internal boundary conditions exist that may prevent the data breakpoint from being captured.

Implication: When this erratum occurs, a data breakpoint will not be captured.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD3. MOV CR3 Performs Incorrect Reserved Bit Checking When in PAE Paging

Problem: The MOV CR3 instruction should perform reserved bit checking on the upper unimplemented address bits. This checking range should match the address width reported by CPUID instruction 0x8000008. This erratum applies whenever PAE is enabled.

Implication: Software that sets the upper address bits on a MOV CR3 instruction and expects a fault may fail. This erratum has not been observed with commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.



AD4. Incorrect Access Controls to MSR_LASTBRANCH_0_FROM_LIP MSR Registers

Problem: When an access is made to the MSR_LASTBRANCH_0_FROM_LIP MSR register, an expected #GP fault may not happen.

Implication: A read of the MSR_LASTBRANCH_0_FROM_LIP MSR register may not cause a #GP fault.

Workaround: None identified

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD5. FXRSTOR May Not Restore Non-canonical Effective Addresses on Processors with Intel® 64 architecture Enabled

Problem: If an x87 data instruction has been executed with a non-canonical effective address, FXSAVE may store that non-canonical FP Data Pointer (FDP) value into the save image. An FXRSTOR instruction executed with 64-bit operand size may signal a General Protection Fault (#GP) if the FDP or FP Instruction Pointer (FIP) is in non-canonical form.

Implication: When this erratum occurs, Intel 64 enabled systems may encounter an unintended #GP fault.

Workaround: Software should avoid using non-canonical effective addressing in 64 enabled processors. BIOS can contain a workaround for this erratum removing the unintended #GP fault on FXRSTOR.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD6. A Push of ESP That Faults May Zero the Upper 32 Bits of RSP

Problem: In the event that a push ESP instruction, that faults, is executed in compatibility mode, the processor will incorrectly zero upper 32-bits of RSP.

Implication: A Push of ESP in compatibility mode will zero the upper 32-bits of RSP. Due to this erratum, this instruction fault may change the contents of RSP. This erratum has not been observed in commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD7. Checking of Page Table Base Address May Not Match the Address Bit Width Supported by the Platform

Problem: If the page table base address, included in the page map level-4 table, page-directory pointer table, page-directory table or page table, exceeds the physical address range supported by the platform (e.g. 36-bit) and it is less than the implemented address range (e.g. 40-bit), the processor does not check if the address is invalid.

Implication: If software sets such invalid physical address in those tables, the processor does not generate a page fault (#PF) upon access to that virtual address, and the access results in an incorrect read or write. If BIOS provides only valid physical address ranges to the operating system, this erratum will not occur.

Workaround: BIOS must provide valid physical address ranges to the operating system.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD8. With TF (Trap Flag) Asserted, FP Instruction That Triggers an Unmasked FP Exception May Take Single Step Trap before Retirement of Instruction

Problem: If an FP instruction generates an unmasked exception with the EFLAGS.TF=1, it is possible for external events to occur, including a transition to a lower power state. When resuming from the lower power state, it may be possible to take the single step trap before the execution of the original FP instruction completes.

Implication: A Single Step trap will be taken when not expected.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD9. BTS (Branch Trace Store) and PEBS (Precise Event Based Sampling) May Update Memory outside the BTS/PEBS Buffer

Problem: If the BTS/PEBS buffer is defined such that:

- The difference between BTS/PEBS buffer base and BTS/PEBS absolute maximum is not an integer multiple of the corresponding record sizes
- BTS/PEBS absolute maximum is less than a record size from the end of the virtual address space
- The record that would cross BTS/PEBS absolute maximum will also continue past the end of the virtual address space

A BTS/PEBS record can be written that will wrap at the 4G boundary (IA32) or 2^{64} boundary (Intel 64 mode), and write memory outside of the BTS/PEBS buffer.

Implication: Software that uses BTS/PEBS near the 4G boundary (IA32) or 2^{64} boundary (Intel 64 mode), and defines the buffer such that it does not hold an integer multiple of records can update memory outside the BTS/PEBS buffer.

Workaround: Define BTS/PEBS buffer such that BTS/PEBS absolute maximum minus BTS/PEBS buffer base is integer multiple of the corresponding record sizes as recommended in the IA-32 Intel® Architecture Software Developer's Manual, Volume 3.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD10. Control Register 2 (CR2) Can be Updated during a REP MOVSt/STOS Instruction with Fast Strings Enabled

Problem: Under limited circumstances while executing a REP MOVSt/STOS string instruction, with fast strings enabled, it is possible for the value in CR2 to be changed as a result of an interim paging event, normally invisible to the user. Any higher priority architectural event that arrives and is handled while the interim paging event is occurring may see the modified value of CR2.

Implication: The value in CR2 is correct at the time that an architectural page fault is signaled. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD11. REP STOS/MOVS Instructions with RCX $\geq 2^{32}$ May Cause a System Hang

Problem: In IA-32e mode using Intel 64-enabled processors, executing a repeating string instruction with the iteration count greater than or equal to 2^{32} and a pending event may cause the REP STOS/MOVS instruction to live lock and hang.

Implication: When this erratum occurs, the processor may live lock and result in a system hang. Intel has not observed this erratum with any commercially available software.

Workaround: Do not use strings larger than 4 GB.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD12. A 64-Bit Value of Linear Instruction Pointer (LIP) May be Reported Incorrectly in the Branch Trace Store (BTS) Memory Record or in the Precise Event Based Sampling (PEBS) Memory Record

Problem: On a processor supporting Intel® 64,

- If an instruction fetch wraps around the 4G boundary in Compatibility Mode, the 64-bit value of LIP in the BTS memory record will be incorrect (upper 32 bits will be set to FFFFFFFFh when they should be 0).
- If a PEBS event occurs on an instruction whose last byte is at memory location FFFFFFFFh, the 64-bit value of LIP in the PEBS record will be incorrect (upper 32 bits will be set to FFFFFFFFh when they should be 0).

Implication: Intel has not observed this erratum on any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD13. Two Correctable L2 Cache Errors in Close Proximity May Cause a System Hang

Problem: If two correctable L2 cache errors are detected in close proximity to each other, a livelock may occur as a result of the processor being unable to resolve this condition.

Implication: When this erratum occurs, the processor may livelock and result in a system hang. Intel has only observed this erratum while injecting cache errors in simulation..

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD14. Processor May Hang with a 25% or Less STPCLK# Duty Cycle

Problem: If a system de-asserts STPCLK# at a 25% or less duty cycle and the processor thermal control circuit (TCC) on-demand clock modulation is active, the processor may hang. This erratum does not occur under the automatic mode of the TCC.

Implication: When this erratum occurs, the processor may hang.

Workaround: If use of the on-demand mode of the processor's TCC is desired in conjunction with STPCLK# modulation, then assure that STPCLK# is not asserted at a 25% duty cycle.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD15. Machine Check Exceptions May not Update Last-Exception Record MSRs (LERs)

Problem: If a system de-asserts STPCLK# at a 25% or less duty cycle and the processor thermal control circuit (TCC) on-demand clock modulation is active, the processor may hang. This erratum does not occur under the automatic mode of the TCC.

Implication: When this erratum occurs, the LER may not contain information relating to the machine check exception. They will contain information relating to the exception prior to the machine check exception

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD16. Writing the Local Vector Table (LVT) when an Interrupt is Pending May Cause an Unexpected Interrupt

Problem: If a local interrupt is pending when the LVT entry is written, an interrupt may be taken on the new interrupt vector even if the mask bit is set.

Implication: An interrupt may immediately be generated with the new vector when a LVT entry is written, even if the new LVT entry has the mask bit set. If there is no Interrupt Service Routine (ISR) set up for that vector the system will GP fault. If the ISR does not do an End of Interrupt (EOI) the bit for the vector will be left set in the in-service register and mask all interrupts at the same or lower priority.

Workaround: Any vector programmed into an LVT entry must have an ISR associated with it, even if that vector was programmed as masked. This ISR routine must do an EOI to clear any unexpected interrupts that may occur. The ISR associated with the spurious vector does not generate an EOI, therefore the spurious vector should not be used when writing the LVT.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD17. At a Bus Ratio of 13:1, RCNT and Address Parity May be Incorrect

Problem: In a system running at the 13:1 bus ratio, RCNT[0] (ADDR# [28], phase b) may report incorrect information.

Implication: RCNT[0] may contain incorrect information and cause address parity machine check errors.

Workaround: Address parity should be disabled and RCNT information should be ignored at the bus ratio of 13:1.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD18. IRET under Certain Conditions May Cause an Unexpected Alignment Check Exception

Problem: In IA-32e mode, it is possible to get an Alignment Check Exception (AC#) on the IRET instruction even though alignment checks were disabled at the start of the IRET. This can only occur if the IRET instruction is returning from CPL3 code to CPL3 code. IRETs from CPL0/1/2 are not affected. This erratum can occur if the EFLAGS value on the stack has the AC flag set, and the interrupt handler's stack is misaligned. In IA-32e mode, RSP is aligned to a 16-byte boundary before pushing the stack frame.

Implication: In IA-32e mode, under the conditions given above, an IRET can get an AC# even if alignment checks are disabled at the start of the IRET. This erratum can only be observed with a software generated stack frame.

Workaround: Software should not generate misaligned stack frames for use with IRET.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD19. L2 Cache ECC Machine Check Errors May be erroneously Reported after an Asynchronous RESET# Assertion

Problem: Machine check status MSRs may incorrectly report the following L2 Cache ECC machine-check errors when cache transactions are in-flight and RESET# is asserted:

- Instruction Fetch Errors (IA32_MC2_STATUS with MCA error code 153)
- L2 Data Write Errors (IA32_MC1_STATUS with MCA error code 145)

Implication: Uncorrected or corrected L2 ECC machine check errors may be erroneously reported. Intel has not observed this erratum on any commercially available system.

Workaround: When a real run-time L2 Cache ECC Machine Check occurs, a corresponding valid error will normally be logged in the IA32_MC0_STATUS register. BIOS may clear IA32_MC2_STATUS and/or IA32_MC1_STATUS for these specific errors when IA32_MC0_STATUS does not have its VAL flag set.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD20. Using 2M/4M Pages When A20M# Is Asserted May Result in Incorrect Address Translations

Problem: An external A20M# pin if enabled forces address bit 20 to be masked (forced to zero) to emulate real-address mode address wraparound at 1 megabyte. However, if all of the following conditions are met, address bit 20 may not be masked:

- paging is enabled
- a linear address has bit 20 set
- the address references a large page
- A20M# is enabled

Implication: When A20M# is enabled and an address references a large page the resulting translated physical address may be incorrect. This erratum has not been observed with any commercially available operating system.

Workaround: Operating systems should not allow A20M# to be enabled if the masking of address bit 20 could be applied to an address that references a large page. A20M# is normally only used with the first megabyte of memory.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD21. Writing Shared Unaligned Data that Crosses a Cache Line without Proper Semaphores or Barriers May Expose a Memory Ordering Issue

Problem: Software which is written so that multiple agents can modify the same shared unaligned memory location at the same time may experience a memory ordering issue if multiple loads access this shared data shortly thereafter. Exposure to this problem requires the use of a data write which spans a cache line boundary.

Implication: This erratum may cause loads to be observed out of order. Intel has not observed this erratum with any commercially available software or system.

Workaround: Software should ensure at least one of the following is true when modifying shared data by multiple agents:

- The shared data is aligned
- Proper semaphores or barriers are used in order to prevent concurrent data accesses

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD22. The IA32_MC0_STATUS and IA32_MC1_STATUS Overflow Bit is not set when Multiple Un-correctable Machine Check Errors Occur at the Same Time

Problem: When two enabled MC0/MC1 un-correctable machine check errors are detected in the same bank in the same internal clock cycle, the highest priority error will be logged in IA32_MC0_STATUS / IA32_MC1_STATUS register, but the overflow bit may not be set.

Implication: The highest priority error will be logged and signaled if enabled, but the overflow bit in the IA32_MC0_STATUS/ IA32_MC1_STATUS register may not be set.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD23. Processor May Fault When the Upper 8 Bytes of Segment Selector Is Loaded from a Far Jump through a Call Gate via the Local Descriptor Table

Problem: In IA-32e mode of the Intel 64 processor, control transfers through a call gate via the Local Descriptor Table (LDT) that uses a 16-byte descriptor, the upper 8-byte access may wrap and access an incorrect descriptor in the LDT. This only occurs on an LDT with a LIMIT>0x10008 with a 16-byte descriptor that has a selector of 0xFFFC.

Implication: In the event this erratum occurs, the upper 8-byte access may wrap and access an incorrect descriptor within the LDT, potentially resulting in a fault or system hang. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AD24. The Processor May Issue Front Side Bus Transactions up to 6 Clocks after RESET# is Asserted

Problem: The processor may issue transactions beyond the documented 3 Front Side Bus (FSB) clocks and up to 6 FSB clocks after RESET# is asserted in the case of a warm reset. A warm reset is where the chipset asserts RESET# when the system is running.

Implication: The processor may issue transactions up to 6 FSB clocks after the RESET# is asserted

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AB25. Front Side Bus Machine Checks May be Reported as a Result of On-Going Transactions during Warm Reset

Problem: Processor Front Side Bus (FSB) protocol/signal integrity machine checks may be reported if the transactions are initiated or in-progress during a warm reset. A warm reset is where the chipset asserts RESET# when the system is running.

Implication: The processor may log FSB protocol/signal integrity machine checks if transactions are allowed to occur during RESET# assertions.

Workaround: BIOS may clear FSB protocol/signal integrity machine checks for systems/chipsets which do not block new transactions during RESET# assertions.

Status: For the steppings affected, see the *Summary Tables of Changes*

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Specification Changes

The Specification Changes listed in this section apply to the following documents:

- *Intel® Celeron® D Processor 300 Sequence – On 65nm Process in the 775-Land Package Datasheet*

All Specification Changes will be incorporated into a future version of the appropriate Celeron® D processor documentation.

AD1. VTT_SEL Signal Specification change

The following text is an updated description of VTT_SEL signal in the *Intel® Celeron® D Processor on the 65 nm process Electrical, Mechanical, and Thermal Specifications*

- VTT_SEL is moved from “Open Drain Signals” to “Signals with No RTT” in Table 2-7 (Signal Characteristics)
- The signal description for VTT_SEL has been updated to include “This land is connected internally in the package to VTT” in Table 5-3 (Signal Description (Sheet 1 to 9))

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Specification Clarifications

The Specification Clarifications listed in this section apply to the following documents:

- *Intel® Celeron® D Processor 300 Sequence – On 65nm Process in the 775-Land Package Datasheet*

All Specification Clarifications will be incorporated into a future version of the appropriate Celeron® D processor documentation.

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Documentation Changes

The Documentation Changes listed in this section apply to the following documents:

- *Intel® Celeron® D Processor 300 Sequence – On 65nm Process in the 775-Land Package Datasheet*

All Documentation Changes will be incorporated into a future version of the appropriate Celeron® D processor documentation.

Note: Documentation changes for *IA-32 Intel® Architecture Software Developer's Manual* volumes 1, 2A, 2B, 3A, and 3B will be posted in a separate document *IA-32 Intel® Architecture Software Developer's Manual Documentation Changes*. Follow the link below to become familiar with this file.

<http://developer.intel.com/design/pentium4/specupdt/252046.htm>

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